Automated Pulsar Data Collector

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The pulsar data collector is a self-contained automated subsystem for the DSS 13 Automation Demonstration. It relieves the 900-series computer from much of the software previously used for data collection. The pulsar data collector is a high speed, periodic signal sampler and integrator which has demonstrated faster operation and higher resolution than existing devices.

I. Introduction

The automated pulsar receiver (Ref. 1) in conjunction with the pulsar data collector are fully programmable subsystems for the Pulsar Automation System at DSS 13. The pulsar receiver is a self-contained, 30 MHz-to-baseband receiver with three selectable predetection bandwidths, a diode power detector, an attenuator, and a variable postdetection filter.

The pulsar data collector is a self-contained, periodic signal sampler and integrator, interfaced with an XDS 900-series computer. The data collector uses a high speed (4 μs conversion time) 12-bit analog-to-digital (A-D) converter. Once the pulsar parameters are programmed into the receiver and the data collector, the computer is free to carry on other tasks as the data collector takes the data and stores them in its own memory. Upon completion, the data collector signals the computer that the observation has ended.

II. The Problem

Limits of the present pulsar timer (Ref. 2) and its implementation as a data collector are its low speed and resolution, its heavy reliance on software and its need for large amounts of computer memory space. With DSS 13 automation, large observation programs and memory allocated to data storage exhaust present memory space in existing 900-series computers. Also, with the current pulsar observing system, it is not possible to increase the resolution of the observations while maintaining phase.

The new pulsar data collector is self-contained with its own memory, high speed transistor-transistor logic (TTL), and Schottky logic control elements. It can maintain phase when parameters are changed to expand the resolution of the observation. It has no operator controls and can be programmed by any 900-series computer.

III. Hardware Implementation

Figure 1 is a block diagram of the new pulsar data collector presently installed at DSS 13 and controlled by the XDS 930 computer. The data collector may be used with any 900-series computer without any hardware modifications. The station 1-s tick (1 pulse/s) and a frequency synthesizer are used to establish the precise timing for the data collector.

There are two single-instruction Energize Output M (EOM) codes used to program the pulsar data collector from the 930 computer. Both EOM codes are manually set with dual-in-line switches within the data collector. This allows changing of the instruction codes easily and makes the data collector compatible with any 900-series computer.

One EOM is used for control. When it is followed by the proper Parallel Output (POT) word from the computer, it sets up the register pointer or starts the data collector in one of three modes: initial-start, start-on-next-major-cycle-clearing-memory, and start-on-next-major-cycle-not-clearing-memory. Initial-start starts the data collector on the next 1-s tick (1 pulse/s).

The second EOM is used for data transfer. The following POT or Parallel Input (PIN) word causes the transfer of a 24-bit word from the computer to the register pointed to in the data collector, or from the data collector register to the computer, respectively.

The register pointer operates in four modes and sets up the condition for transfer of data between the computer and the registers. The memory address counter (A) and the memory (M) are considered registers. In the first mode, the register pointer will point only to the register designated in the POT word following the control EOM and will not change until commanded by a new control EOM POT sequence. In the second mode, the register pointer will increment to the next register in sequence after a data transfer POT has occurred. It will not increment beyond the M position. In the M position, the increment after POT or PIN will refer to the memory address counter (A). The third mode is the same as the second except the increment will occur after a data transfer PIN. In the fourth mode, the increment will occur after a data transfer POT or PIN and is used for memory testing.

There are eight binary registers in the data collector. The maximum number of bits for each register is as follows:

X	16
Y	24
Δ	24
L	24
N	16
D	16
A	13
M	24

The data stored in the X and Y buffer-hold registers must be the 2's complement of the actual number used as the divisor for determining minor and major cycle pulses from the frequency synthesizer input. The Δ register stores the delay of the number of minor cycle pulses to wait after a major cycle pulse before starting data collection. The L register holds the number of minor cycle pulses delayed plus the number of minor cycle pulses to be used as data points. The N register holds the number of major cycles to be observed. The D hold register cannot be programmed directly but is cleared by every initial start command. The D register holds the number of major cycle pulses that have occurred between the end of one observation and the start of the next observation.

The X and Y counters are used as modulo n dividers where n max for X = 2^{16} and n max for Y = 2^{24}. The X counter sets the number of frequency synthesizer pulses for each minor cycle pulse; the Y counter sets the number of minor cycle pulses for each major cycle pulse.

The major cycle length is generally set to the period or repetition rate of the observed pulsar. The minor cycle pulses are then the number of samples during this period. The X and Y counters are not stopped between observations, and their reference values are changed only at the very beginning of a major cycle. New values from the computer are kept in buffer registers. As long as the product of X and Y is kept the same, phase will be maintained between observations.

A 16-bit up/down counter is used as the N counter with the major cycle pulses being counted. During observation, the N counter counts down from the number loaded into the N hold register. When the count reaches zero, a computer interrupt is fired to signal completion of the observation and the counter starts counting up. At the beginning of the next observation, the number counted up to in the N counter is transferred to the D hold register. With each new start command the N counter is reset to a down counter with the value of the N hold register in it.

The Δ and L counter is cleared by the major cycle pulse and counts up with each minor cycle pulse; the maximum count is 2^{24}. This counter, in conjunction with two 24-bit comparators and the Δ and the L hold registers, controls the start and end of data collection and the storage of the data in memory. The value of Δ determines at which minor cycle pulse (relative to the beginning of the major cycle) data are first taken and stored in the first memory location. It can be 0 to 2^{24}. The value of L should be the value of Δ plus the number of samples to be stored in memory. Data are taken at each minor cycle pulse between Δ and L. The value of the number of samples may be from 1 to 8000, which is the minimum and maximum size of the memory.

Pulsars only emit significant radiation during about 1/10 of the period. By using new values in the X, Y, Δ and L hold registers determined from full-period observations, one can take all the observations during a limited fraction of the period, thus increasing the resolution without destroying the phase of the observed data.

The memory address counter is controlled by the start and end pulses from Δ and L comparators while data are being collected. When the memory is being controlled by the computer, the address counter is set to an effective memory location when the register pointer is pointing to the A register. The address counter automatically increments at the end of a POT or PIN when the register pointer is pointing to the M register. During data collection, the address counter always starts at zero and stops at L. The memory automatically cycles through starting at zero with each new major cycle pulse.

The 8K × 24-bit memory is comprised of two Standard Memories, Inc. 8K × 18-bit stand alone memory modules. Every third bit in each module is not used, giving 48,000 spare bits in each module. The output of the memory (M_o) is in 2's complement.

During the first scan of data after an initial–start or start-on-the-next-major-cycle-with-clear-memory, the First-N-Inhibit prevents the old data within the memory from being added to the new data. This effectively clears the memory by storing only the new data in each memory location. During subsequent scans, the contents of the effective memory location are called up, added to the new data point, stored in the adder-hold-register and written back in the effective memory location for each minor cycle pulse.

The A-D converter is a Datel ADC-N-12C 12–bit, 2's complement bipolar converter, with a sample and hold module ahead of it. The maximum conversion rate is 4 μs. The data collector is independent of the converter and may be used with new higher speed devices as they become available.

The PIN data multiplexer (MUX) allows data from any of the registers or memory to be selectively read into the 930 computer. The register being read is dependent on the register pointer position after a control EOM, as described earlier.

IV. Software

Table 1 shows the EOM codes and POT bit positions for control of the Automated Pulsar Receiver. Also included is a skip-if-signal-not-set (SKS) test for automatic mode. When the receiver is in the local mode the computer has no control of the functions.

Table 2 shows the EOM codes and POT bit positions for control and data transfer of the pulsar data collector. An interrupt to the 930 computer is also supplied to signal completion of an observation.

V. Conclusion

The automated pulsar receiver and data collector are subsystems for the DSS 13 automation demonstration. These subsystems have been installed, tested, and are now operational.

The first test results for PSR 0329-54 and PSR 0833-45 shown in Fig. 2 give an example of the high resolution available with the pulsar data collector. The horizontal axis is time and is 5,000 samples long. The vertical axis is the power density of the pulsar proportional to the integration number and average received power. Pulsar 0329 has an average rate with a period of 700 ms. Plot 1 shows the results of two, full-period integrations. Plot 2 shows the results of taking the same number of observations during the first half of the period only.

Pulsar 0833 has a fast rate with a period of 83 ms. Plot 3 shows a full period observation after an initial start. Plot 4 is an example of applying the expansion technique, showing greater detail of the pulsar emission. Data points were taken every 8.3 μs.

References

1. Foster, C. F., "Automated Pulsar Receiver," in *The Deep Space Network Progress Report 42-20*, pp. 135-138, Jet Propulsion Laboratory, Pasadena, Calif., Apr. 15, 1974.

2. Slekys, A., "A New Pulsar Timer," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. XIII, pp. 133-138, Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1973.

Table 1. Automated pulsar receiver control codes

Instruction	Code	Followed by instruction	Function
SKS	31015	–	Skip if receiver in remote
EOM	30515	–	Reset and disable remote outputs
EOM	31115	–	Set and enable remote outputs
EOM	30115	POT	Attenuator set
EOM	30215	POT	Predetection bandwidth set
EOM	30415	POT	Postdetection bandwidth set

POT Word Format

Attenuator	Six bits, right justified. Minimum attenuation = 01 octal, maximum attenuation = 77 octal, 0.5 dB steps from 0 to 31.5 dB.
Predetection Bandwidth	Two bits, right justified. Octal: 0 = 10 MHz bandwidth; 1 = Wide bandwidth; 2 = 1 MHz bandwidth
Postdetection Bandwidth	Fifteen bits, right justified. Minimum time constant = 00001 octal, maximum time constant = 77777 octal, 1μs steps from 0 to 31 ms.

Table 2. Automated pulsar data collector control codes

Instruction	Code[a]	Followed by instruction	Function
EOM	30016	POT	Control, sets up register point and command instructions.
EOM	30116	POT	Data transfer, from computer to data collector register indicated in control word.
EOM	30116	PIN	Data transfer, from data collector register indicated in control word to the computer.

Control POT Word Format

Octal number	Function
01	X register point
02	Y register point
03	Δ register point
04	L register point
05	N register point
06	D register point
07	A register point
00	M register point
10[b]	Increment after POT
20[b]	Increment after PIN
040	Initial start
100	Start on next major cycle pulse clearing memory
300	Start on next major cycle pulse not clearing memory

Data Transfer Word Format

Register	Maximum word length
X	16 bits, right justified
Y	24 bits
Δ	24 bits
L	24 bits
N	16 bits, right justified
D	16 bits, right justified
A	13 bits, right justified
M	24 bits

[a]May be changed by dual-in-line switches in data collector.

[b]May be mixed with preceding control words.

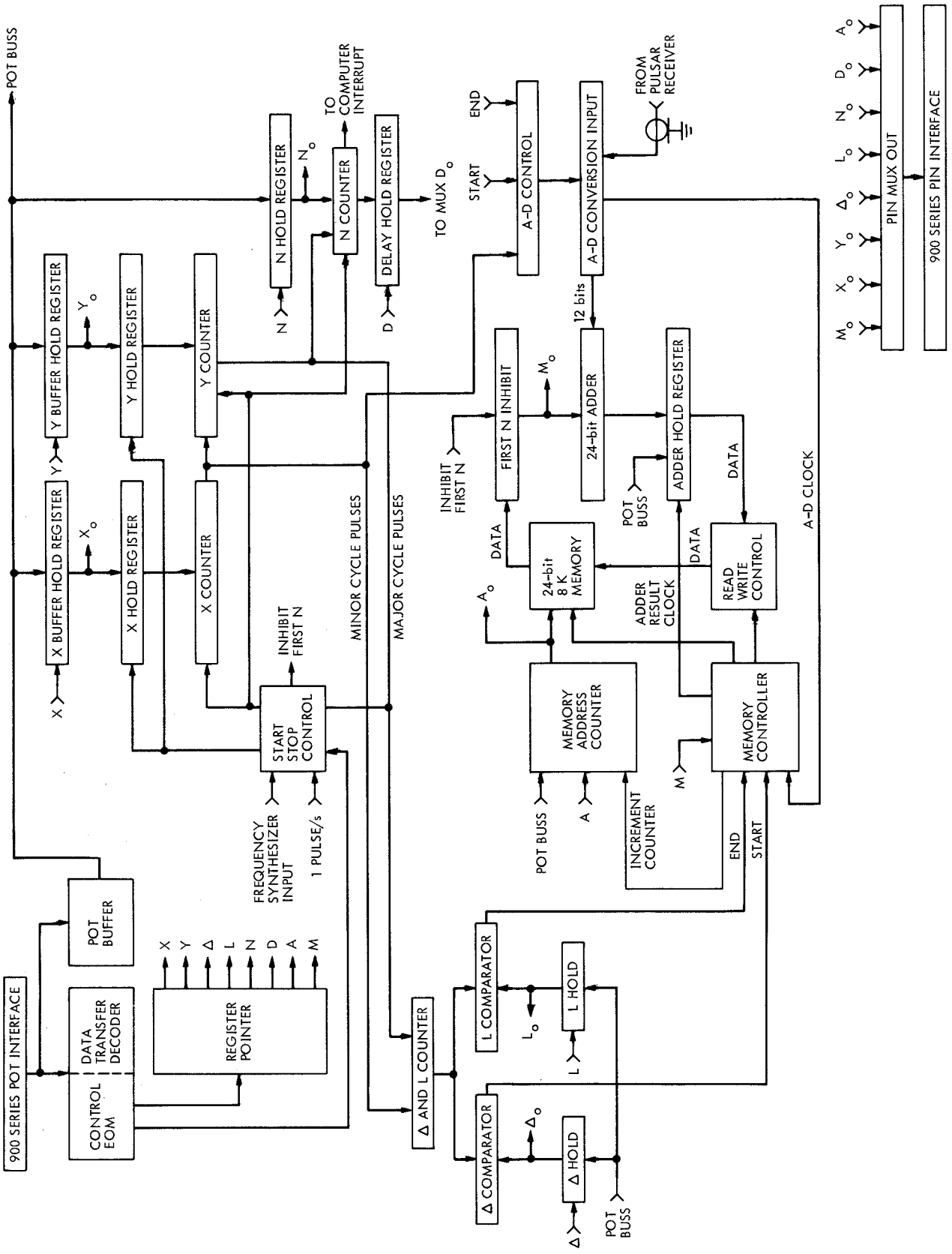

Fig. 1. Pulsar data collector block diagram

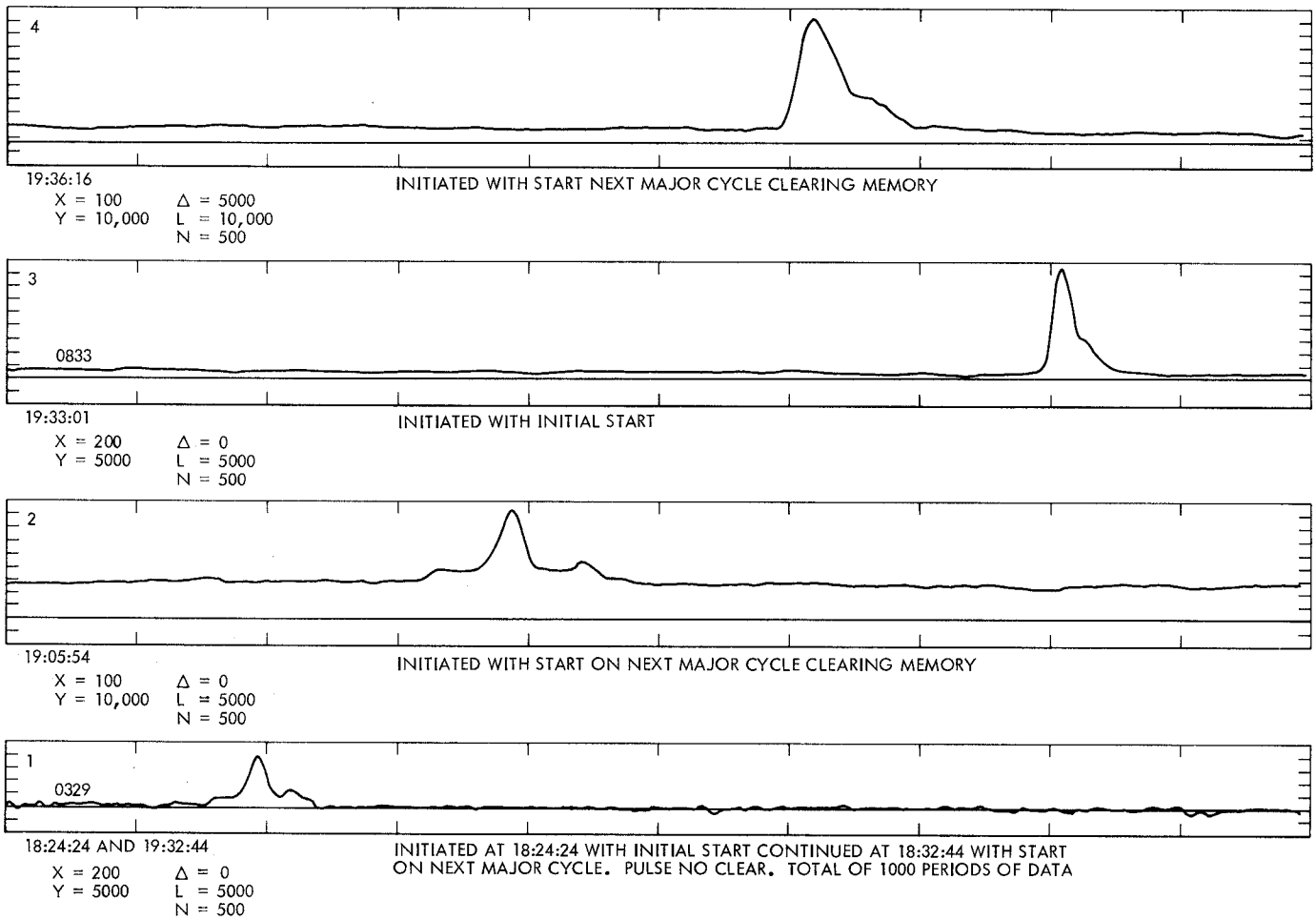

Fig. 2. Pulsar data plots, July 26, 1974